

## WE CLAIM:

## 1. An integrated circuit device comprising:

an embedded memory having addressable memory locations;

5 a built-in self-test (BIST) circuit coupled electrically to said memory and operable so as to perform consecutive test operations upon said memory locations of said memory;

an access time measuring circuit coupled  
10 electrically to said memory and said BIST circuit and operable so as to generate an access time signal corresponding to access time of one of said memory locations that is currently being tested by said BIST circuit; and

15 a built-in detecting circuit coupled electrically to said access time measuring circuit, said detecting circuit monitoring a maximum value of the access time signals generated by said access time measuring circuit during the consecutive test operations, and being  
20 operable so as to output a maximum access time signal upon completion of the consecutive test operations.

## 2. The integrated circuit device as claimed in Claim 1, wherein said detecting circuit includes:

a time signal converter coupled electrically to said  
25 access time measuring circuit for converting the access time signal generated during each of the consecutive test operations into a corresponding compared signal;

and

a peak value detector coupled electrically to said time signal converter for comparing the compared signal with a reference signal and for updating the reference signal so as to correspond with the compared signal according to result of comparison therebetween;

the maximum value of the access time signals being determined from the reference signal upon completion of the consecutive test operations.

3. The integrated circuit device as claimed in Claim 2, wherein each of the consecutive test operations includes a first read procedure for reading first test data of one of said memory locations that is currently being tested, a write procedure that follows said first read procedure for writing second test data which is the inverse of the first test data in said one of said memory locations that is currently being tested, and a second read procedure that follows said write procedure for reading the second test data of said one of said memory locations that is currently being tested, the access time signal for one of said memory locations that is currently being tested by said BIST circuit being generated during said second read procedure of the test procedure therefor,

wherein said time signal converter includes a control unit for enabling conversion operation of said time signal converter during a time period starting from

generation of the access time signal associated with a current tested one of said memory locations and ending before generation of the access time signal associated with a next tested one of said memory locations, and

5        wherein said peak value detector includes a control device for enabling update operation of said peak value detector during the time period starting from generation of the access time signal associated with the current tested one of said memory locations and ending before  
10       generation of the access time signal associated with the next tested one of said memory locations.

4. The integrated circuit device as claimed in Claim 3, wherein said time signal converter further includes a signal integrator coupled electrically to said access  
15       time measuring circuit for converting the access time signal generated during each of the consecutive test operations into the corresponding compared signal, said control unit including a switch connected across said signal integrator and operable so as to discharge said  
20       signal integrator when the conversion operation of said signal integrator is disabled.

5. The integrated circuit device as claimed in Claim 3, wherein said peak value detector further includes:  
      a storage element for storing the reference signal;  
25       a comparator coupled electrically to said storage element and said time signal converter for comparing the compared signal from said time signal converter with

the reference signal from said storage element;

a buffer coupled electrically to said time signal converter so as to receive the compared signal therefrom; and

5 a switch interconnecting said storage element and said buffer, said switch being connected to and being controlled by said comparator so as to make or break electrical connection between said buffer and said storage element according to result of comparison made  
10 by said comparator.

6. The integrated circuit device as claimed in Claim 5, wherein said control device includes a logic gate interconnecting said switch and said comparator and operable so as to inhibit said comparator from  
15 controlling said switch when the update operation of said peak value detector is disabled.

7. The integrated circuit device as claimed in Claim 5, wherein said peak value detector further includes a reset element connected across said storage element and operable so as to discharge said storage element.  
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8. The integrated circuit device as claimed in Claim 5, wherein said detecting circuit further includes an output signal converter coupled electrically to said storage element and operable so as to output the maximum  
25 access time signal upon completion of the consecutive test operations.

9. The integrated circuit device as claimed in Claim 8, wherein said detecting circuit further includes:

5 a first control switch coupled electrically to said storage element, said comparator and said switch, said first control switch operable so as to break electrical connection between said storage element and each of said comparator and said switch upon completion of the consecutive test operations; and

10 a second control switch coupled electrically to said storage element and said output signal converter and operable so as to make electrical connection between said storage element and said output signal converter upon completion of the consecutive test operations.

10. A detecting circuit adapted for detecting maximum memory access time internally of an integrated circuit device, the integrated circuit device including

an embedded memory having addressable memory locations,

20 a built-in self-test (BIST) circuit coupled electrically to the memory and operable so as to perform consecutive test operations upon the memory locations of the memory, and

25 an access time measuring circuit coupled electrically to the memory and the BIST circuit and operable so as to generate an access time signal corresponding to access time of one of the memory locations that is currently being tested by the BIST

circuit,

said detecting circuit comprising:

a time signal converter adapted to be coupled electrically to the access time measuring circuit and operable so as to convert the access time signal generated by the access time measuring circuit during each of the consecutive test operations into a corresponding compared signal; and

a peak value detector coupled electrically to said time signal converter for comparing the compared signal with a reference signal and for updating the reference signal so as to correspond with the compared signal according to result of comparison therebetween;

wherein a maximum value of the access time signals generated during the consecutive test operations is determined from the reference signal upon completion of the consecutive test operations.

11. The detecting circuit as claimed in Claim 10, each of the consecutive test operations including a first read procedure for reading first test data of one of the memory locations that is currently being tested, a write procedure that follows the first read procedure for writing second test data which is the inverse of the first test data in said one of the memory locations that is currently being tested, and a second read procedure that follows the write procedure for reading the second test data of said one of the memory locations

that is currently being tested, the access time signal for one of the memory locations that is currently being tested by the BIST circuit being generated during the second read procedure of the test operation therefor, wherein:

said time signal converter includes a control unit for enabling conversion operation of said time signal converter during a time period starting from generation of the access time signal associated with a current tested one of the memory locations and ending before generation of the access time signal associated with a next tested one of the memory locations; and

said peak value detector includes a control device for enabling update operation of said peak value detector during the time period starting from generation of the access time signal associated with the current tested one of the memory locations and ending before generation of the access time signal associated with the next tested one of the memory locations.

12. The detecting circuit as claimed in Claim 11, wherein said time signal converter further includes a signal integrator adapted to be coupled electrically to the access time measuring circuit for converting the access time signal generated during each of the consecutive test operations into the corresponding compared signal, said control unit including a switch connected across said signal integrator and operable so as to discharge

said signal integrator when the conversion operation of said signal integrator is disabled.

13. The detecting circuit device as claimed in Claim 11, wherein said peak value detector further includes:

5       a storage element for storing the reference signal;

      a comparator coupled electrically to said storage element and said time signal converter for comparing the compared signal from said time signal converter with the reference signal from said storage element;

10       a buffer coupled electrically to said time signal converter so as to receive the compared signal therefrom; and

      a switch interconnecting said storage element and said buffer, said switch being connected to and being  
15       controlled by said comparator so as to make or break electrical connection between said buffer and said storage element according to result of comparison made by said comparator.

14. The detecting circuit as claimed in Claim 13, wherein  
20       said control device includes a logic gate interconnecting said switch and said comparator and operable so as to inhibit said comparator from controlling said switch when the update operation of said peak value detector is disabled.

25       15. The detecting circuit as claimed in Claim 13, wherein said peak value detector further includes a reset element connected across said storage element and operable so



as to discharge said storage element.

16. The detecting circuit as claimed in Claim 13, further comprising an output signal converter coupled electrically to said storage element and operable so as to output a maximum access time signal corresponding to the reference signal upon completion of the consecutive test operations.

17. The detecting circuit as claimed in Claim 16, further comprising:

10 a first control switch coupled electrically to said storage element, said comparator and said switch, said first control switch being operable so as to break electrical connection between said storage element and each of said comparator and said switch upon completion of the consecutive test operations; and

15 a second control switch coupled electrically to said storage element and said output signal converter and operable so as to make electrical connection between said storage element and said output signal converter upon completion of the consecutive test operations.

20 18. A method for detecting maximum memory access time internally of an integrated circuit device, the integrated circuit device including an embedded memory having addressable memory locations, a built-in self-test (BIST) circuit coupled electrically to the memory and operable so as to perform consecutive test operations upon the memory locations of the memory, and

an access time measuring circuit coupled electrically to the memory and the BIST circuit and operable so as to generate an access time signal corresponding to access time of one of the memory locations that is currently being tested by the BIST circuit,

each of the consecutive test operations including a first read procedure for reading first test data of one of the memory locations that is currently being tested, a write procedure that follows the first read procedure for writing second test data which is the inverse of the first test data in said one of the memory locations that is currently being tested, and a second read procedure that follows the write procedure for reading the second test data of said one of the memory locations that is currently being tested,

the access time signal for one of the memory locations that is currently being tested by the BIST circuit being generated during the second read procedure of the test operation therefor,

said method comprising the steps of:

- a) monitoring a maximum value of the access time signals generated by the access time measuring circuit during the consecutive test operations; and
- b) outputting a maximum access time signal upon completion of the consecutive test operations.

19. The method as claimed in Claim 18, wherein said step

a) includes the sub-steps of:

a-1) converting the access time signal generated by the access time measuring circuit during each of the consecutive test operations into a corresponding compared signal; and

5 a-2) comparing the compared signal with a reference signal and updating the reference signal so as to correspond with the compared signal according to result of comparison therebetween;

10 wherein the maximum value of the access time signals is determined based on the reference signal upon completion of the consecutive test operations.

20. The method as claimed in Claim 19, wherein each of sub-steps a-1) and a-2) is performed during a time period starting from generation of the access time signal associated with a current tested one of said memory locations and ending before generation of the access time signal associated with a next tested one of said memory locations.

21. The method as claimed in Claim 20, wherein the maximum access time signal outputted in said step b) is an analog signal.

22. The method as claimed in Claim 20, wherein the maximum access time signal outputted in said step b) is a digital signal.

25 23. A detecting circuit adapted for detecting maximum memory access time internally of an integrated circuit device, the integrated circuit device including an

embedded memory having addressable memory locations,  
a built-in self-test (BIST) circuit coupled  
electrically to the memory and operable so as to perform  
consecutive test operations upon the memory locations  
5 of the memory, and an access time measuring circuit  
coupled electrically to the memory and the BIST circuit  
and operable so as to generate an access time signal  
corresponding to access time of one of the memory  
locations that is currently being tested by the BIST  
10 circuit,

each of the consecutive test operations including  
a first read procedure for reading first test data of  
one of the memory locations that is currently being tested,  
a write procedure that follows the first read procedure  
15 for writing second test data which is the inverse of  
the first test data in said one of the memory locations  
that is currently being tested, and a second read  
procedure that follows the write procedure for reading  
the second test data of said one of the memory locations  
20 that is currently being tested,

the access time signal for one of the memory locations  
that is currently being tested by the BIST circuit being  
generated during the second read procedure of the test  
operation therefor,

25 said detecting circuit comprising:

monitoring means, adapted to be coupled electrically  
to the access time measuring circuit, for monitoring

a maximum value of the access time signals generated by the access time measuring circuit during the consecutive test operations; and

5        output means, coupled electrically to said monitoring means, for outputting a maximum access time signal upon completion of the consecutive test operations;

10        wherein said monitoring means is enabled during a time period starting from generation of the access time signal associated with a current tested one of said memory locations and ending before generation of the access time signal associated with a next tested one of said memory locations.